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MC88110

Advance Information

MC88110 Second Generation RISC Microprocessor Hardware Specifications

The MC88110 is the second implementation of the 88000 family of reduced instruction set computer (RISC) microprocessors. The Symmetric Superscalar™ design of the MC88110 allows sustained performance to approach the peak performance capability. This document contains electrical characteristics, pin grid array pinouts, mechanical drawings, and standard marking specifications for the MC88110.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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1.1 MC88110 Microprocessor Electrical Specifications

This section provides both the AC and DC electrical specifications and the JTAG characteristics for the MC88110.

1.1.1 DC Electrical Characteristics

Table 1 provides the maximum ratings for the MC88110.

Table 1. Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit
Supply voltage	V_{dd}	–0.3 to 7.0	V
Input voltage	V_{in}	–0.8 to 7.0	V
Maximum operating junction temperature	T_J	85	°C
Storage temperature range	T_{stg}	–55 to 150	°C

Note: Functional operating conditions are given in DC electrical specifications. Operation beyond the maximum listed may affect device reliability or cause permanent damage to the device.

Table 2 provides the DC electrical characteristics for the MC88110.

Table 2. DC Electrical Characteristics

Characteristic	Comments	Symbol	Min	Max	Unit
Input high voltage	All inputs except the CLK	V_{IH}	2	V_{dd}	V
Input low voltage	All inputs except the CLK	V_{IL}	GND	0.8	V
CLK input high voltage		CV_{IH}	2.4	V_{dd}	V
CLK input low voltage		CV_{IL}	GND	0.5	V
Input leakage current $GND \le V_{IN} \le V_{dd}$		I_{in}	—	2	µa
Hi-Z (off-state) leakage current @ 0.5/2.4 V		I_{TSI}	—	2	µa
Signal low input current V_{IL} = 0.8 V and V_{IH} = 2.0 V	TMS, TDI, $\overline{TRST}$	I_{IL}, I_{IH}	50	500	µa
Output high voltage I_{OH} = 20 ma		V_{OH}	2.4	—	V
Output low voltage I_{OL} = 20 ma		V_{OL}	—	0.5	V
Capacitance[1] V_{in} = 0 V, f = 1 MHz		C_{in}	—	15	pF
Typical power dissipation (ambient)	50 MHz 40 MHz	P_D	— —	10 8.5	W W

Note: [1]Capacitance is periodically sampled rather than 100% tested.

1.1.2 AC Electrical Characteristics

Table 3 through Table 5 provide information on AC timing characteristics for the MC88110.

Table 3. Clock AC Timing Specifications

Vdd = 5.0 V dc ± 5%, GND = 0 V dc

Num.	Note	Characteristic	40 MHz		50 MHz		Unit
			Min	Max	Min	Max	
		Frequency of operation	33	40	40	50	MHz
1		CLK cycle time	25	30	20	25	ns
2	1	CLK rise time	—	2	—	2	ns
3	1	CLK fall time	—	2	—	2	ns
4		CLK duty cycle measured at 1.4 V	40	60	40	60	%
4a		CLK pulse width high measured at 1.4 V	10	22	8	15	ns
4b		CLK pulse width low measured at 1.4 V	10	22	8	15	ns

Note: 1. While the rise and fall times for the CLK input will be measured from 0.8 to 2.0 volts, the CLK signal is expected to swing from 0.5 to 2.4 volts.

Table 4. Input AC Timing Specifications

Vdd = 5.0 V dc ± 5%, GND = 0 V dc, T_J Max = 85 °C

Num.	Notes 1, 3	Characteristic	40 MHz		50 MHz		Unit
			Min	Max	Min	Max	
5		Data, byte parity in valid to CLK (setup)	12	—	9	—	ns
6		CLK to data, byte parity in invalid (hold)	–4	—	–3	—	ns
7		$\overline{\text{PTA}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{TRTRY}}$, $\overline{\text{AACK}}$ valid to CLK (setup)	12	—	9	—	ns
7A		$\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$ valid to CLK (setup)	12	—	8	—	ns
8		CLK to $\overline{\text{PTA}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{TRTRY}}$, $\overline{\text{AACK}}$, $\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$ in invalid (hold)	–4	—	–3	—	ns
9		$\overline{\text{DBG}}$ and $\overline{\text{BG}}$ valid to CLK (setup)	12	—	9	—	ns
10		CLK to $\overline{\text{DBG}}$ and $\overline{\text{BG}}$ invalid (hold)	–2	—	–1	—	ns
11	4	Address valid to CLK (setup)	6	—	4	—	ns
12	4	CLK to address invalid (hold)	2	—	2	—	ns
13		$\overline{\text{SR}}$ in valid to CLK (setup)	12	—	9	—	ns
14		CLK to $\overline{\text{SR}}$ in invalid (hold)	–2	—	–1	—	ns
15		$\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ in valid to CLK (setup)	12	—	9	—	ns

Table 4. Input AC Timing Specifications (Continued)

Vdd = 5.0 V dc ± 5%, GND = 0 V dc, T_J Max = 85 °C

Num.	Notes 1, 3	Characteristic	40 MHz		50 MHz		Unit
			Min	Max	Min	Max	
16		CLK to $\overline{ABB}$ and $\overline{DBB}$ in invalid (hold)	–2	—	–1	—	ns
17	2	$\overline{NMI}$, $\overline{INT}$, $\overline{RST}$, and $\overline{DBUG}$ valid to CLK (setup)	6	—	4	—	ns
18		CLK to $\overline{NMI}$, $\overline{INT}$, $\overline{RST}$, and $\overline{DBUG}$ invalid (hold)	2	—	2	—	ns

Notes:

1. All input specs are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the 1.4 V of the input CLK. Input timings are measured at the pin.
2. These signals will pass through one clock of debounce circuitry internal to the processor before being functionally recognized. They need to be held asserted for at least the full span of one clock cycle.
3. These numbers are for operation at the frequency specified in the column heading only.
   For reduced frequency operation of a 50-MHz part, apply the following formulas to these specs:
   #5, 7, 9, 13, 15: Min = $T_{cyc}/4 + 4$ ns
   #6, 8: Min = $-T_{cyc}/4 + 2$ ns
   #7A: Min = $T_{cyc}/4 + 3$ ns
   #10, 14, 16: Min = $-T_{cyc}/4 + 4$ ns
   For reduced frequency operation of a 40-MHz part, apply the following formulas to these specs:
   #5, 7, 7A, 9, 13, 15: Min = $T_{cyc}/4 + 5.75$ ns
   #6, 8: Min = $-T_{cyc}/4 + 2.25$ ns
   #10, 14, 16: Min = $-T_{cyc}/4.25 + 4$ ns
4. These control signals have timing that coincides with address: $\overline{TBST}$, R/$\overline{W}$, $\overline{INV}$, $\overline{GBL}$.

Table 5. Output AC Timing Specifications

Vdd = 5.0 V dc ± 5%, GND = 0 V dc, T_J Max = 85 °C, C_L = (see note 1)

Num.	Notes 1,5	Characteristic	40 MHz		50 MHz		Unit
			Min	Max	Min	Max	
19	4	CLK to address valid	5	17	4	15	ns
20	4	CLK to address invalid	5	—	4	—	ns
21	2	CLK to $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$ asserted, negated	0	11	0	10	ns
22		CLK to data, byte parity, $\overline{BPE}$ out valid	5	17	4	15	ns
23		CLK to data, byte parity, $\overline{BPE}$ out invalid	5	—	4	—	ns
24		CLK to data, byte parity, $\overline{BPE}$ out hi-impedance	5	15	4	12	ns
25	4	CLK to address hi-impedance	5	15	4	12	ns
26		CLK to $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$ hi-impedance	11	20	9	17	ns
27		CLK to output lo-impedance	5	—	4	—	ns
27A		CLK to $\overline{ABB}$, $\overline{DBB}$, $\overline{TS}$ lo-impedance	0	—	0	—	ns
28		CLK to $\overline{BR}$ asserted	0	11	0	10	ns

Table 5. Output AC Timing Specifications (Continued)

Vdd = 5.0 V dc ± 5%, GND = 0 V dc, T_J Max = 85 °C, C_L = (see note 1)

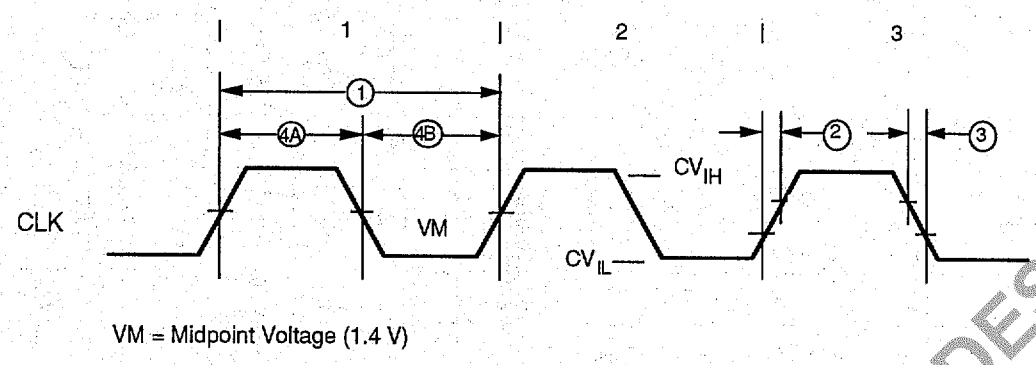
Num.	Notes 1,5	Characteristic	40 MHz		50 MHz		Unit
			Min	Max	Min	Max	
29		CLK to $\overline{BR}$ negated	0	11	0	10	ns
30		CLK to $\overline{SSTAT0}$ and $\overline{SSTAT1}$ asserted	0	11	0	10	ns
31	3	CLK to $\overline{SSTAT0}$ and $\overline{SSTAT1}$ negated	—	17	—	15	ns
32		CLK to $\overline{SSTAT0}$ and $\overline{SSTAT1}$ hi-impedance	17	27	14	22	ns
33		CLK to PSTAT2–PSTAT0 valid	5	17	4	15	ns
33A		CLK to PSTAT2–PSTAT0 invalid	5	—	4	—	ns

Notes:

1. All outputs except $\overline{TS}$ and $\overline{SSTAT1}$–$\overline{SSTAT0}$ are specified with an output load of 50 pF and a line length of 6 inches. The $\overline{TS}$ and $\overline{SSTAT1}$–$\overline{SSTAT0}$ signals are specified with a load of 60 pF and a line length of 6 inches. All output timing specifications assume a board impedance in the range of 50–90 ohms and a dielectric constant in the range of 2 to 6. All output specs are measured from the 1.4 V of the input CLK to the TTL level (0.8 or 2.0 V) of the signal in question. Outputs are measured both at the pin and at the end of the 6-inch line.
2. The shared outputs $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, $\overline{SSTAT1}$–$\overline{SSTAT0}$ must have pull-up resistors to hold them negated when there is no bus master.
3. Because $\overline{SSTAT0}$ and $\overline{SSTAT1}$ may be asserted by more than one processor, they are negated in a unique fashion. First all processors will three-state for 4 ns, and then the signal will be driven high by all processors. This protocol should prevent driver contention on these signals.
4. These control signals have timing that coincides with address: TSIZ1–TSIZ0, $\overline{TBST}$, TC3–TC0, $\overline{UPA1}$–$\overline{UPA0}$, R/$\overline{W}$, $\overline{LK}$, $\overline{CI}$, $\overline{WT}$, $\overline{INV}$, $\overline{MC}$, $\overline{GBL}$. The $\overline{TS}$, $\overline{ABB}$ and $\overline{DBB}$ signals are asserted $T_{cyc}/4$ prior to address.
5. These numbers are for operation at the frequency specified in the column heading only.
   For reduced frequency operation of a 50-MHz part, apply the following formulas to these specs:
   - #19,20,22,23,24,25,27,33,33A: Min = $T_{cyc}/4 - 1$ ns
   - #19,22,31,33: Max = $T_{cyc}/4 + 10$ ns
   - #24,25: Max = $T_{cyc}/4 + 7$ ns
   - #26: Min = $T_{cyc}/2 - 1$ ns
   - #26: Max = $T_{cyc}/2 + 7$ ns
   - #32: Min = $3T_{cyc}/4 - 1$ ns
   - #32: Max = $3T_{cyc}/4 + 7$ ns

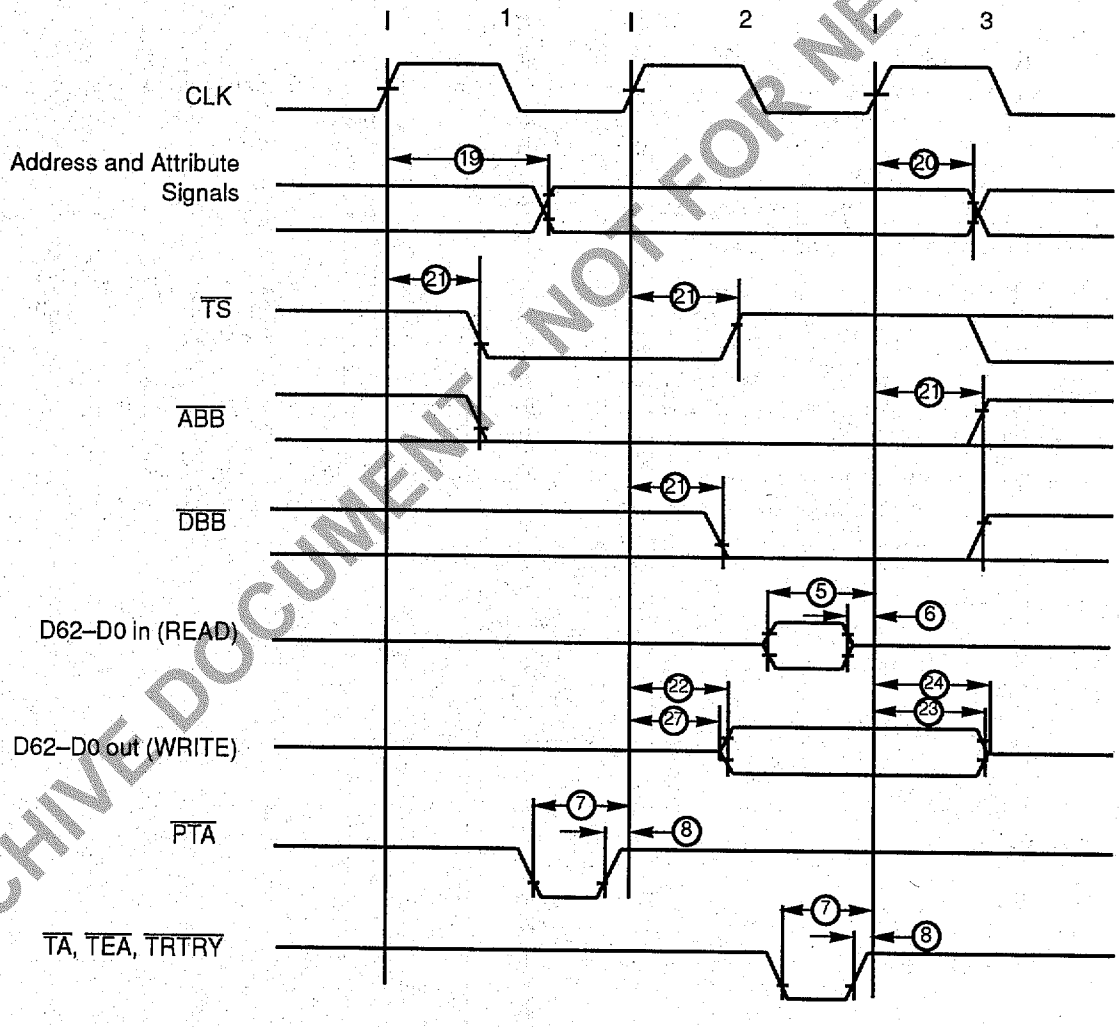
   For reduced frequency operation of a 40-MHz part, apply the following formulas to these specs:
   - #19,20,22,23,24,25,27,33,33A: Min = $T_{cyc}/4 - 1.25$ ns
   - #19,22,31,33: Max = $T_{cyc}/4 + 10.75$ ns
   - #24,25: Max = $T_{cyc}/4 + 8.75$ ns
   - #26: Min = $T_{cyc}/2 - 1.5$ ns
   - #26: Max = $T_{cyc}/2 + 8.5$ ns
   - #32: Min = $3T_{cyc}/4 - 1.75$ ns
   - #32: Max = $3T_{cyc}/4 + 8.25$ ns

Figure 1 through Figure 5 provide a graphical representation of the electrical specifications outlined previously.



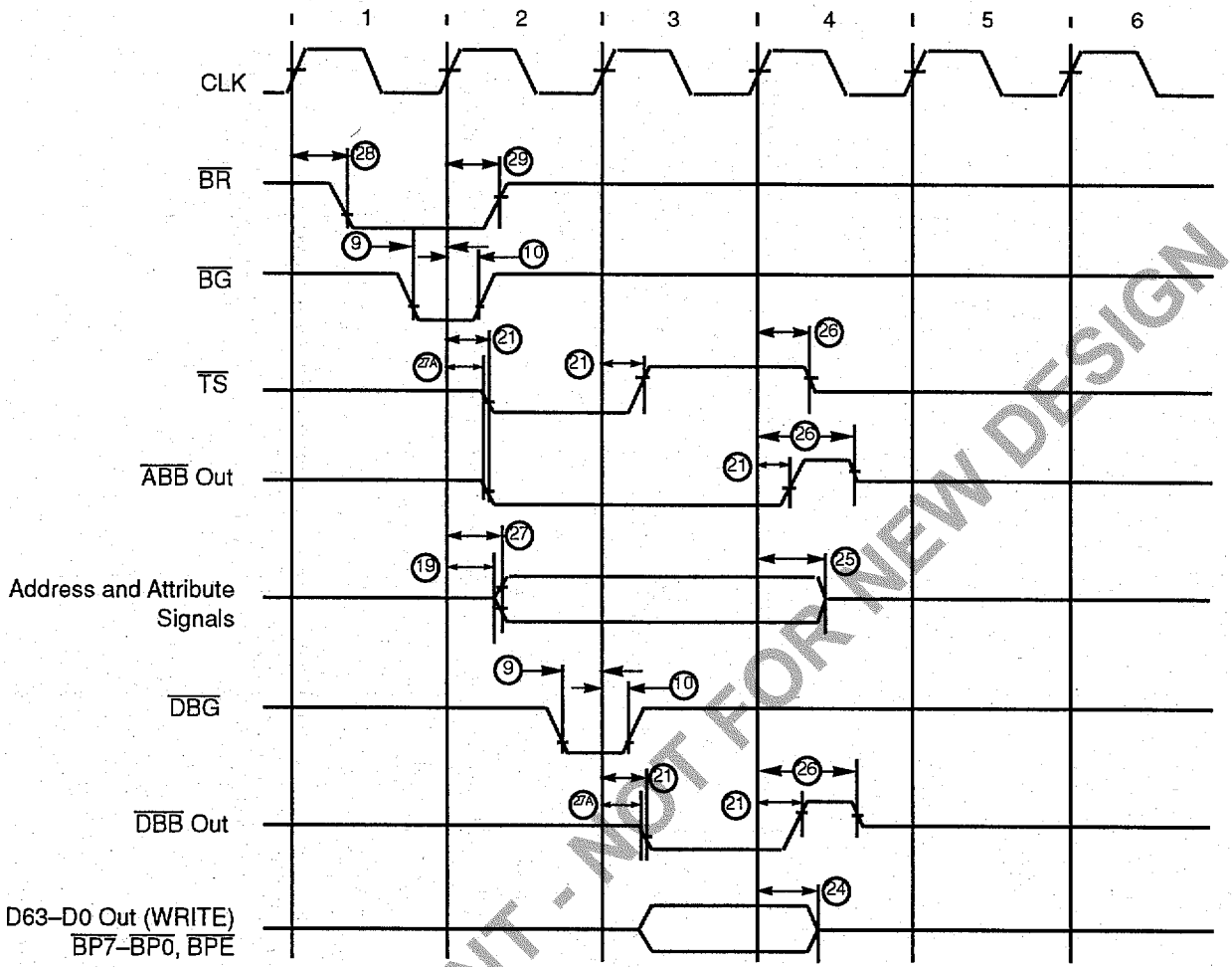
VM = Midpoint Voltage (1.4 V)

Figure 1. Clock Input Timing Diagram



Note: Signals that coincide with addresses and attributes are A31–A0, TSIZ1–TSIZ0, $\overline{\text{TBST}}$, TC2–TC0, $\overline{\text{UPA1}}$–$\overline{\text{UPA0}}$, R/$\overline{\text{W}}$, $\overline{\text{LK}}$, $\overline{\text{CI}}$, $\overline{\text{WT}}$, $\overline{\text{INV}}$, $\overline{\text{MC}}$, and $\overline{\text{GBL}}$.

Figure 2. Read/Write Timing Diagram



Note: Signals that coincide with addresses and attributes are A31–A0, TSIZ1–TSIZ0, TBST, TC2–TC0, UPA1–UPA0, R/W, LK, CI, WT, INV, MC, and GBL.

Figure 3. Bus Arbitration Timing Diagram

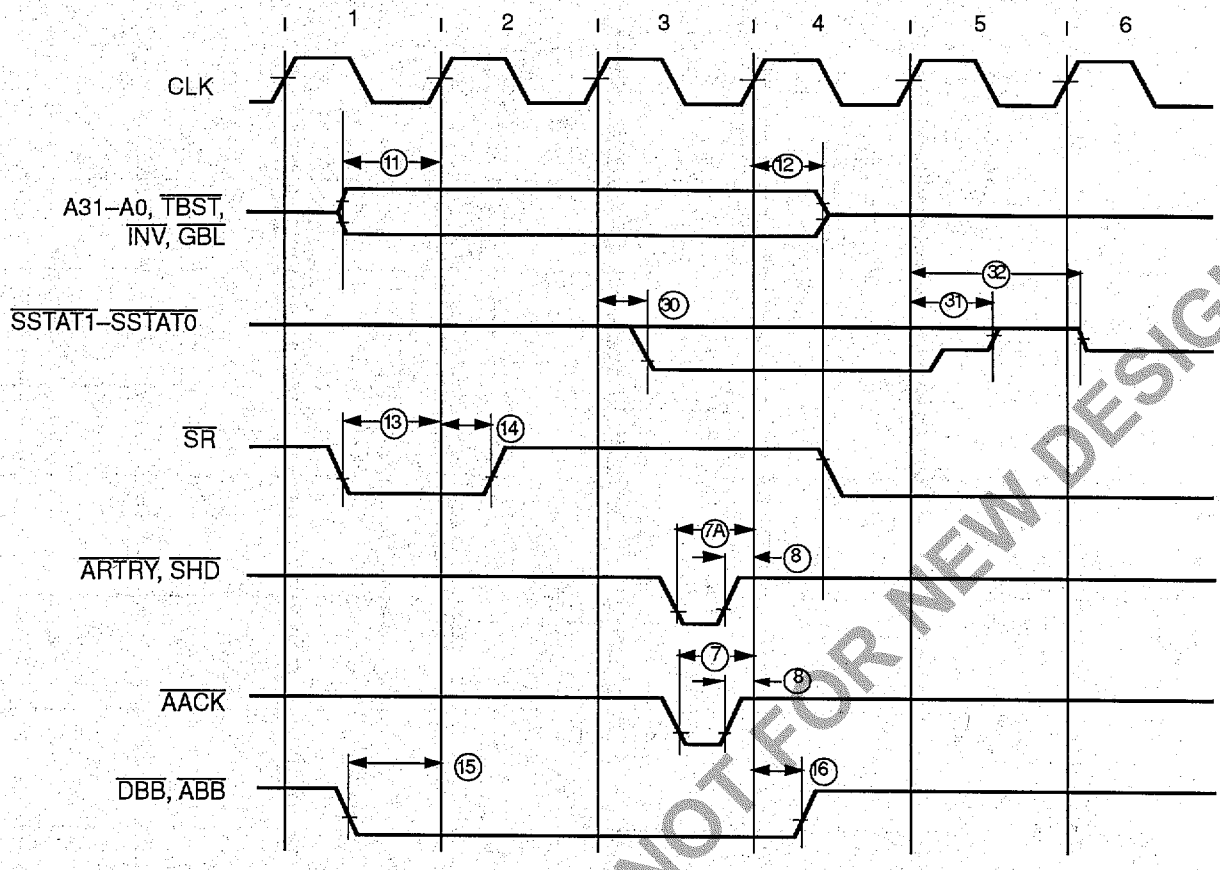


Figure 4. Snoop Timing Diagram

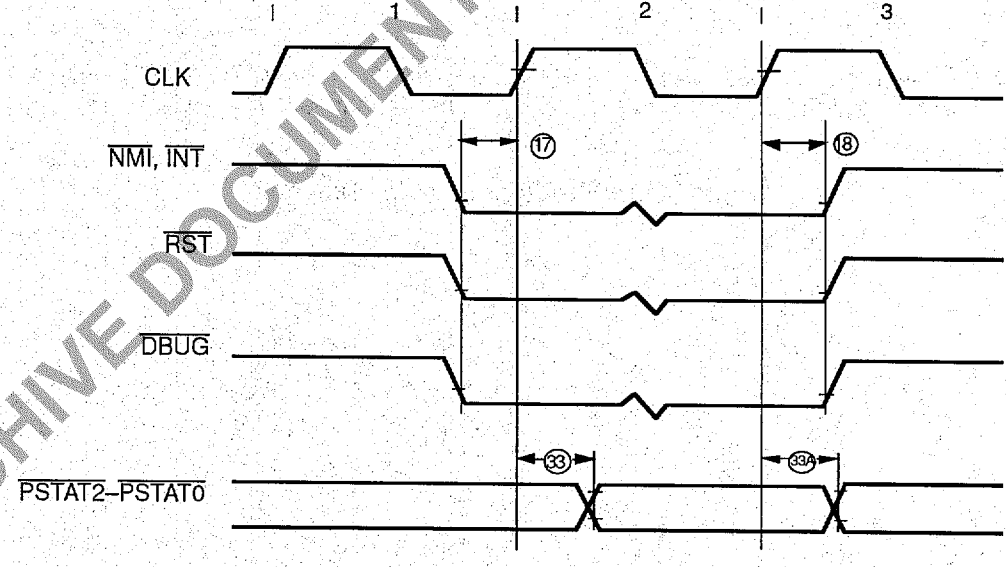


Figure 5. Other Signals Timing Diagram

1.1.3 JTAG AC Timing Specifications

Table 6 provides the JTAG AC timing specifications for the MC88110.

Table 6. JTAG AC Timing Specifications (Independent of SYSCLK)

Num	Characteristic	Min	Max	Unit	Notes
	TCK frequency of operation	0	10	MHz	
1	TCK cycle time	100	—	ns	
2	TCK clock duty cycle measured at 1.4 V	40	60	ns	
3	TCK rise and fall times	0	3	ns	
4	$\overline{\text{TRST}}$ negated setup time to TCK rising edge	30	—	ns	2
5	$\overline{\text{TRST}}$ assert time	20	—	ns	
6	Boundary-scan input data setup time	10	—	ns	3
7	Boundary-scan input data hold time	15	—	ns	3
8	TCK to output data valid	4	35	ns	4
9	TCK to output high impedance	—	35	ns	4
10	TMS, TDI data setup time	10	—	ns	
11	TMS, TDI data hold time	10	—	ns	
12	TCK to TDO data valid	—	20	ns	1
13	TCK to TDO high impedance	3	20	ns	1

Notes:

1. Load capacitance = 20 pF
2. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time guarantees that the specified signal will be recognized on that clock edge.
3. Non-test signal input timing with respect to TCK
4. Non-test signal output timing with respect to TCK

Figure 6 provides the JTAG clock input timing diagram.

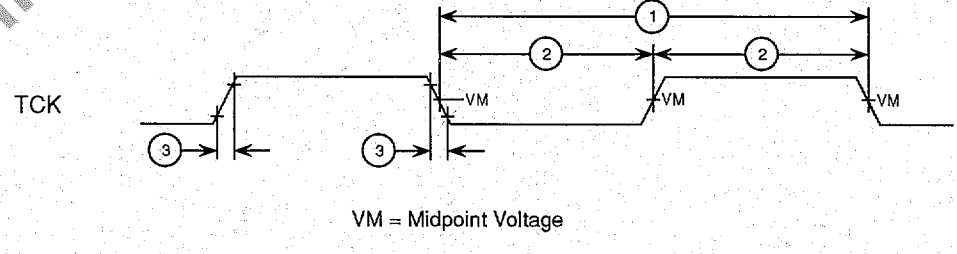


Figure 6. Clock Input Timing Diagram

Figure 7 provides the $\overline{\text{TRST}}$ timing diagram.

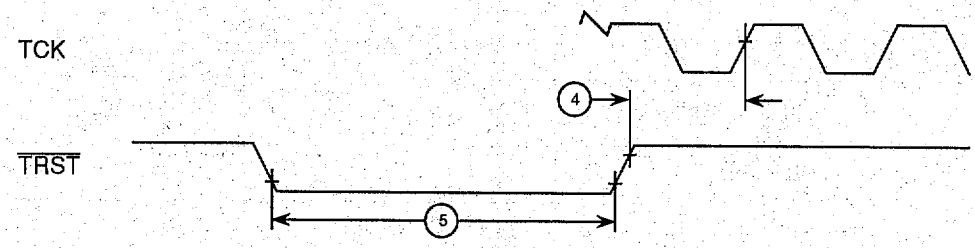


Figure 7. $\overline{\text{TRST}}$ Timing Diagram

Figure 8 provides the boundary-scan timing diagram.

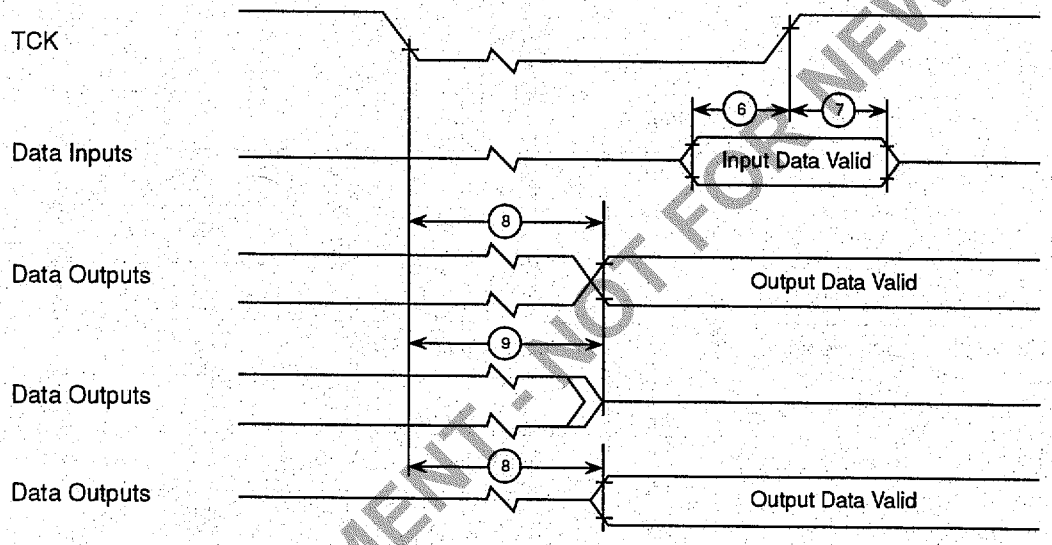


Figure 8. Boundary-Scan Timing Diagram

Figure 9 provides the test access port timing diagram.

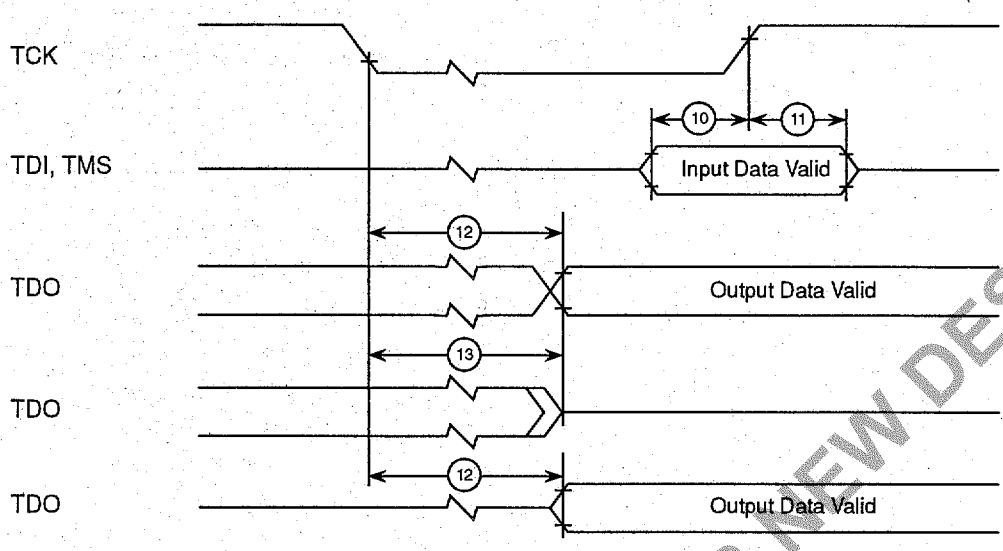
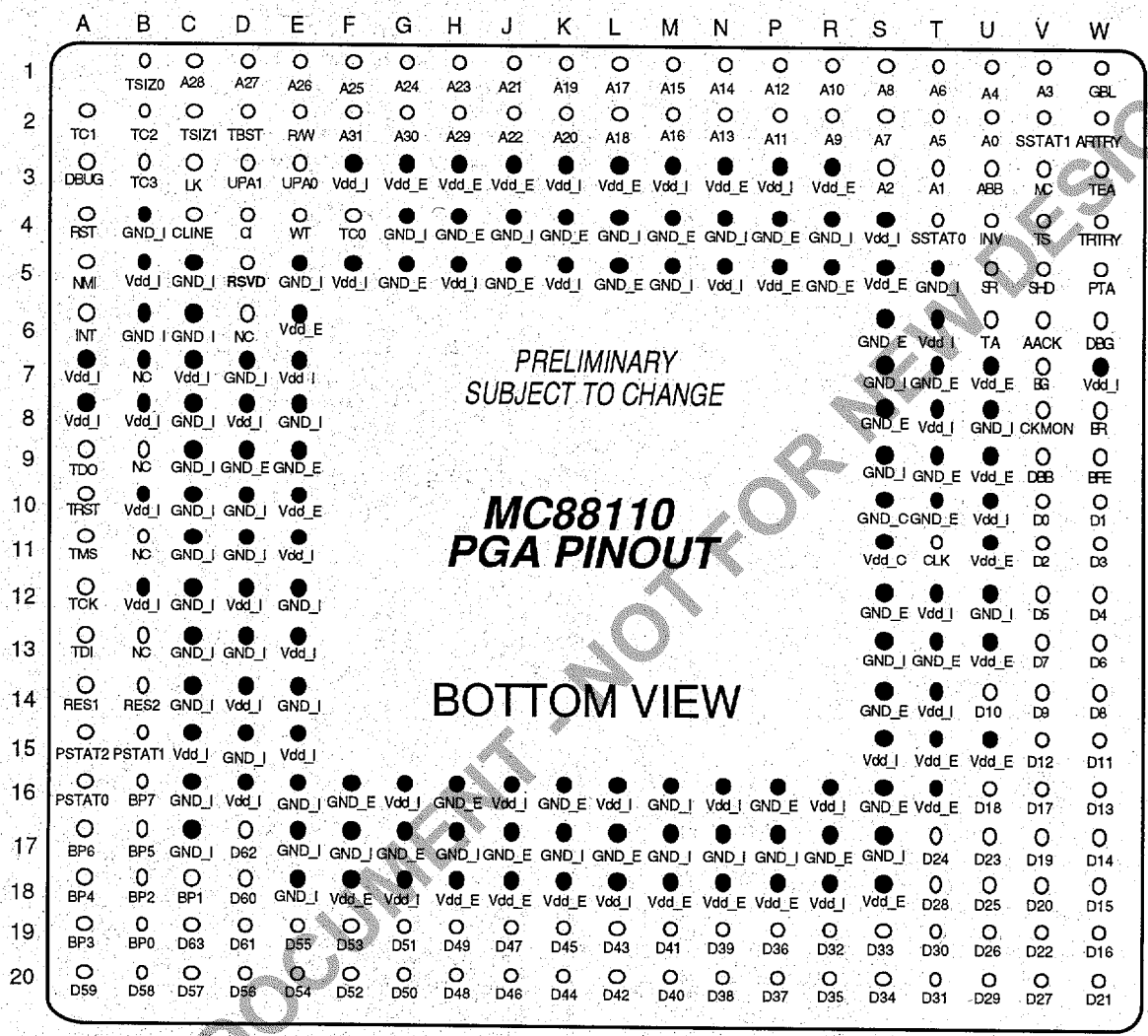


Figure 9. Test Access Port Timing Diagram

1.2 MC88110 Pinout Diagram

The MC88110 is available in a 299-pin package. Figure 10 shows the pin assignments for the MC88110. Power and ground pins are divided into those used for internal signals, external signals and buses, and clocking. These groupings are listed in Table 7.



Notes:

1. NC = Do not connect.
2. CKMON is an output test pin and should be left unconnected.
3. RSVD should be pulled to V_{dd} through a 10K ohm resistor.

Figure 10. MC88110 Processor Pin Assignments

1.3 MC88110 Pinout Listing

Table 7 provides the pinout listing for the MC88110.

Table 7. MC88110 Signals and Pin Locations

Signal	Pin Location
Internal logic V_{dd}	A7, A8, B5, B8, B10, B12, C7, C15, D8, D12, D14, D16, E7, E11, E13, E15, F3, F5, G16, G18, H5, J16, K3, K5, L16, L18, M3, N5, N16, P3, R16, R18, S4, S15, T6, T8, T12, T14, U10, W7
External signals and buses V_{dd}	E6, E10, F18, G3, H3, H18, J3, J18, K18, L3, M18, N3, N18, P5, P18, R3, S5, S18, T16, U7, U9, U11, U13, U15, T15
Clock V_{dd}	S11
Internal logic GND	B4, B6, C5, C6, C8, C9, C10, C11, C12, C13, C14, C16, C17, D7, D10, D11, D13, D15, E5, E8, E12, E14, E16, E17, E18, F17, G4, H17, J4, K17, L4, M5, M16, M17, N4, N17, P17, R4, S7, S9, S13, S17, T5, U8, U12
External signals and buses GND	D9, E9, F16, G5, G17, H4, H16, J5, J17, K4, K16, L5, L17, M4, P4, P16, R5, R17, S6, S8, S12, S14, S16, T7, T9, T10, T13
Clock GND	S10
CLK	T11
A31–A0	F2,G2,H2,C1,D1,E1,F1, G1, H1, J2, J1, K2, K1, L2, L1, M2, M1, N1, N2, P1, P2, R1, R2, S1, S2, T1, T2, U1, V1, S3, T3, U2
$\overline{TS}$	V4
TSIZ1–TSIZ0	C2, B1
R/$\overline{W}$	E2
TC3–TC0	B3, B2, A2, F4
$\overline{LK}$	C3
$\overline{WT}$	E4
$\overline{UPA1}$–$\overline{UPA0}$	D3, E3
$\overline{CI}$	D4
$\overline{MC}$	V3
$\overline{INV}$	U4
$\overline{GBL}$	W1
$\overline{TBST}$	D2
CLINE	C4
PSTAT2–PSTAT0	A15, B15, A16
D63–D0	C19, D17, D19, D18, A20, B20, C20, D20, E19, E20, F19, F20, G19, G20, H19, H20, J19, J20, K19, K20, L19, L20, M19, M20, N19, N20, P20, P19, R20, S20, S19, R19, T20, T19, U20, T18, V20, U19, U18, T17, U17, V19, W20, V18, V17, U16, V16, W19, W18, W17, W16, V15, W15, U14, V14, W14, V13, W13, V12, W12, W11, V11, W10, V10
BP7–BP0	B16, A17, B17, A18, A19, B18, C18, B19

Table 7. MC88110 Signals and Pin Locations (Continued)

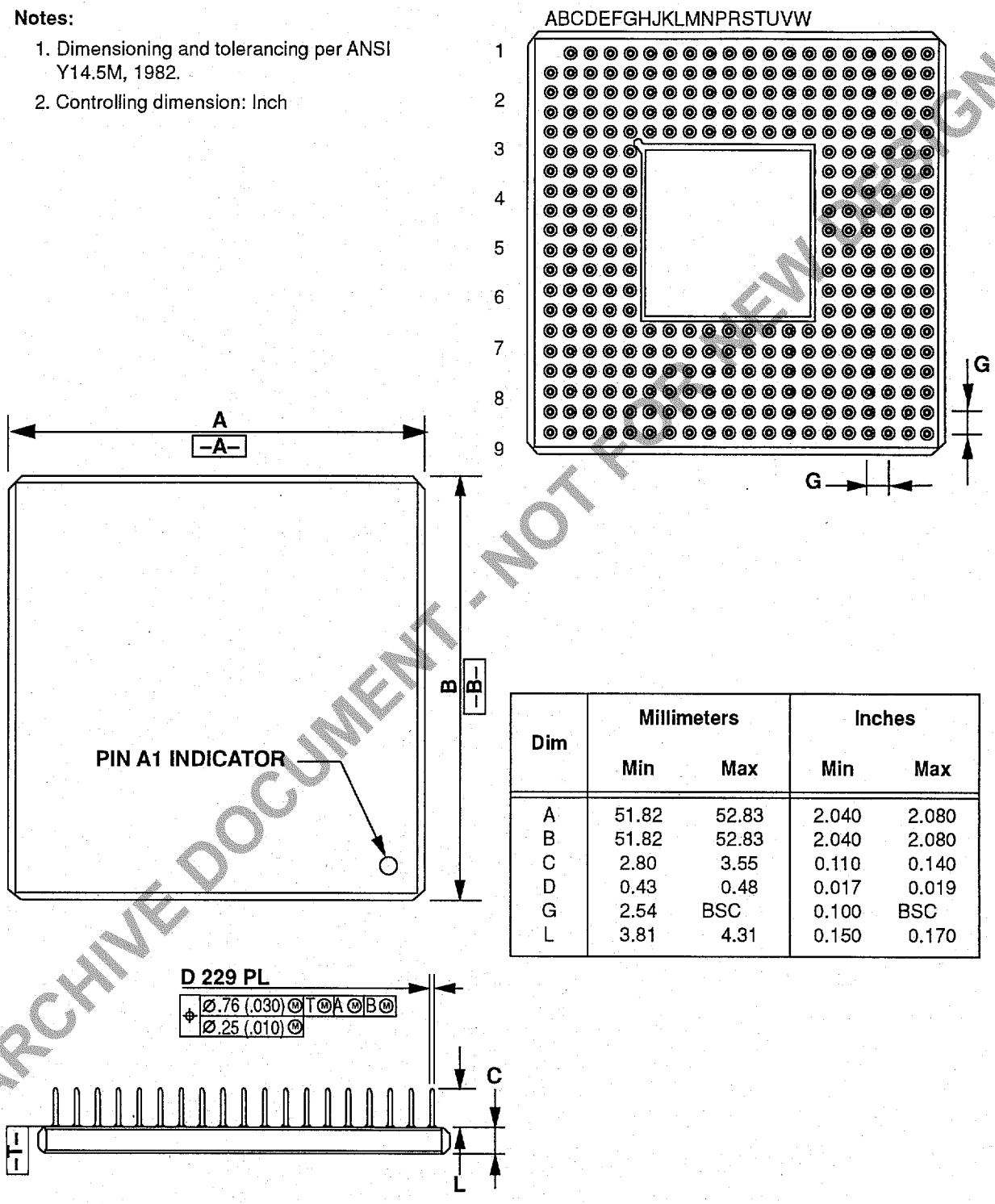
Signal	Pin Location
$\overline{TA}$	U6
$\overline{TEA}$	W3
$\overline{TRTRY}$	W4
$\overline{PTA}$	W5
$\overline{SR}$	U5
$\overline{SSTAT1}$–$\overline{SSTAT0}$	V2, T4
$\overline{ARTRY}$	W2
$\overline{SHD}$	V5
$\overline{AACK}$	V6
$\overline{BG}$	V7
$\overline{BR}$	W8
$\overline{ABB}$	U3
$\overline{DBG}$	W6
$\overline{DBB}$	V9
$\overline{DBUG}$	A3
$\overline{BPE}$	W9
$\overline{NMI}$	A5
$\overline{INT}$	A6
$\overline{RST}$	A4
TDI	A13
TMS	A11
$\overline{TRST}$	A10
TCK	A12
TDO	A9
RES2	B14
RES1	A14
RSVD	D5
CKMON	V8
NC	B7, B9, B11, B13, D6

1.4 MC88110 Mechanical Dimensions

Figure 11 shows the mechanical dimensions for the MC88110.

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: Inch



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	51.82	52.83	2.040	2.080
B	51.82	52.83	2.040	2.080
C	2.80	3.55	0.110	0.140
D	0.43	0.48	0.017	0.019
G	2.54	BSC	0.100	BSC
L	3.81	4.31	0.150	0.170

Figure 11. Mechanical Dimensions of the MC88110

1.5 Standard Marking Specifications

The MC88110 product marking criteria is shown in Figure 12. This information is intended to be used for identification purposes only.

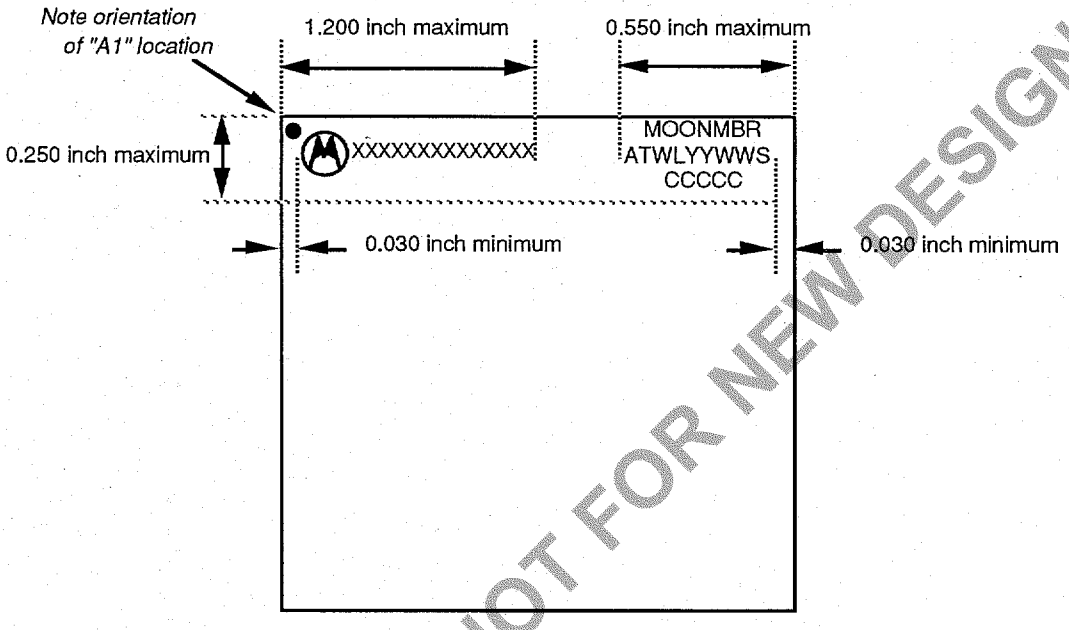


Figure 12. MC88110 Marking Specifications—Illustrated

Notes:

1. The MC88110 is available in a 299-pin, 20 x 20 cavity down pin grid array.
2. (M) = Motorola logo.
   - Logo must be 0.120 inches in size.
   - Logo must be placed as indicated in Figure 12.
   - Bottom of logo must be no further than 0.250 inches from top edge of package.
3. XXXXXXXXXXXXXX—line is reserved for customer part number or Motorola device number.
   - Maximum 14 characters
   - Character size must be 0.060 inches.
4. Motorola logo and customer part number or Motorola device number must be justified as shown.
5. MOONMBR—line is reserved for Motorola mask set number.
   - Maximum 7 characters
   - Character size must be 0.040 inches
   - Top of mark must be no less than 0.030 inches from top edge of package.
6. ATWLYYWWS—line is reserved for Motorola traceability code.
   - Maximum 15 characters
   - Character size must be 0.040 inches.

— There should be a minimum 0.010-inch separation between this line and the MOONMBR line.
— The designator S is reserved for Motorola assembly sublot code—maximum 1 alpha character.
— The first sublot uses the letter 'A'.

7. CCCCC—line is reserved for country of origin (if other than U.S.)
   — Maximum 7 characters
   — Character size must be 0.040 inches.
   — Bottom of mark must be no further than 0.250 inches from top edge of package.
   — There should be a minimum 0.010-inch separation between this line and the ATWLYYWWS line.

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1ATX31204–1 PRINTED IN USA 3/95 IMPERIAL LITHO 12104 3,500 RISC.YGAHAA

MC88110EC/D