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Running the MC88110 in Lockstep

Systems that use two MC88110s in lockstep must take several precautions to guarantee deterministic behavior. First, all inputs, including asynchronous inputs (for example, interrupts) must meet all setup and hold times so that they are recognized on the same clock. Second, the system must ensure that initial decoding of invalid instructions does not affect the timing of one, but not both, of the processors.

Because of the high degree of parallelism in the MC88110, the sequencer performs some initial decoding of instructions before it knows whether the instructions are valid. In some cases, an invalid opcode that is partially decoded can affect the internal timing of the data unit. For instruction cache accesses, the value on the data bus is forwarded to the instruction unit once pretransfer acknowledge (PTA) is asserted. The instruction unit performs some initial decoding regardless of whether the instruction is valid. Therefore, the data bus must be driven with the same data for both processors coincident with and following the assertion of PTA for all instruction cache accesses.

After power-up and before attempting to run in lockstep, the system should enable the caches on both devices, initialize each instruction cache so that they are consistent, and initialize each target instruction cache (TIC) by stepping through a series of branches. Note that it is not sufficient to just invalidate the cache entries; they must be initialized to the same values. One alternative for the instruction cache is to fill it with NOPs (for example, **add r0, r0, r0**). The general register files and the extended register files in both processors should also be initialized to the same values. This can be done very quickly using a series of **or rD, r0, r0** instructions for the general register file and a series of **mov xD, x0** instructions for the extended register file.

Once the instruction cache, TIC, control registers, and register files are consistent on both parts, the two processors can be synchronized and the system can start running in lockstep. One way to synchronize the processors is to assert reset to each device. When coming out of reset, the caches and register files will be unchanged, and the control registers will have their default values. An alternate method is to assert an interrupt signal to both parts at the same time. This will work if both processors are in serial mode (SER in the processor status register is set), both sets of control registers are consistent, the exceptions freeze (EFRZ) and interrupt disable (IND) bits in the processor status register are clear, and both processors are in a loop that branches to itself. In this case, the two processors will begin the exception handler for the interrupt at the same time, and they will continue to operate in lockstep.

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